IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) An ~~computer chip comprising a power supply~~apparatus, comprising:

a chip package;

an integrated circuit electrically connected to the chip package;

chip logic disposed on the integrated circuit; and

a clock tree, disposed on the integrated circuit, that comprises at least one clock driver, wherein power distributed from the power supply to the clock tree is isolated in the chip package from power distributed from the power supply to the chip logic.

2. (Currently Amended) The ~~computer chip~~apparatus of claim 1, further comprising:

a capacitor, wherein power distributed from the power supply to the capacitor is isolated from power distributed from the power supply to the chip logic.

3. (Currently Amended) The ~~computer chip~~apparatus of claim 1, wherein the chip logic comprises at least one logic element.

4. (Canceled)

5. (Currently Amended) The ~~computer chip~~apparatus of claim 1, further comprising:

a first lead through a circuit board to the computer chip, wherein the first lead is used to distribute power from the power supply to the clock tree; and

a second lead through the circuit board to the computer chip, wherein the second lead is used to distribute power from the power supply to the chip logic.

6. (Currently Amended) The ~~computer chip~~apparatus of claim 5, wherein the first lead runs through a chip package, and wherein the second lead runs through the chip package.

7. (Currently Amended) A method for reducing clock skew, comprising:

drawing current from a power supply for chip logic operations conducted on an integrated circuit electrically connected to a chip package; and

drawing current from the power supply for clock tree operations conducted on the integrated circuit,

wherein the current drawn from the power supply for the chip logic operations is isolated in the chip package from the current drawn from the power supply for the clock tree operations.

8. (Original) The method of claim 7, wherein the clock tree comprises a clock generator and at least one clock driver.

9. (Original) The method of claim 7, wherein the chip logic comprises at least one logic element.

10. (Original) The method of claim 7, further comprising:

drawing current from the power supply to decouple noise, wherein the current drawn from the power supply to decouple noise is isolated from the current drawn for the chip logic operations.

11. (Original) The method of claim 7, further comprising:

using separate leads through a chip package to distribute power from the power supply to the clock tree and the chip logic.

12. (Original) The method of claim 7, further comprising:

using separate leads through a circuit board to distribute power from the power supply to the clock tree and the chip logic.